

## Final exam correction

### Exercise 1 : (7 pts)

#### 1/Address Format and Mapping

- Total memory words:  $2^{19} \times 32 = 2^{24}$  words
- Word address size: **24 bits**

#### a. Direct-Mapped Cache

Address Format (24 bits):

- Tag: 16 bits
- Block field: 3 bits
- Word field: 5 bits

Mapping for 0x1E50A4:

- Maps to cache block 5

#### b. Fully Associative Cache

Address Format (24 bits):

- Tag: 19 bits
- Word field: 5 bits

Mapping for 0x1E50A4:

- Can be placed in any of the 8 cache blocks

#### c. Four-Way Set Associative Cache

Address Format (24 bits):

- Number of sets: 8 blocks / 4 ways = 2 sets
- Tag: 18 bits
- Set field: 1 bit
- Word field: 5 bits

Mapping for 0x1E50A4:

- Set field= 1
- Maps to set 1 (can occupy any of 4 blocks in that set 4,5,6, or 7)

#### 2/ a-Direct-Mapped Cache

- Since the block size is 32 words, we can calculate the block number in main memory for each address using the formula:  $\text{Block Number} = \text{Address} \div 32$
- number of blocks in the cache memory =  $2^8 / 32 = 8$
- block number in cache memory =  $\text{Block number} \bmod 8$

Time	0	1	2	3	4	5	6	7	8	9	10	11	12
Address	5469	2085	4126	675	4099	6755	2081	2370	8420	37	544	680	244
Block N° in MM	170	65	128	21	128	211	65	74	263	1	17	21	7
Block N° in MM	<b>2</b>	<b>1</b>	<b>0</b>	<b>5</b>	<b>0</b>	<b>3</b>	<b>1</b>	<b>2</b>	<b>7</b>	<b>1</b>	<b>1</b>	<b>5</b>	<b>7</b>
Block0			<b>128</b>										
Block 1		<b>65</b>	<b>1</b>	<b>17</b>	<b>17</b>	<b>17</b>							
Block 2	<b>170</b>	<b>74</b>	<b>74</b>	<b>74</b>	<b>74</b>	<b>74</b>	<b>74</b>						
Block 3						<b>211</b>							
Block 4													
Block 5				<b>21</b>									
Block 6													
Block 7									<b>263</b>	<b>263</b>	<b>263</b>	<b>263</b>	<b>7</b>
Hit/miss	miss	miss	miss	miss	hit	miss	hit	miss	miss	miss	miss	hit	miss

- **Hits:** 3
- **Misses:** 10
- **Hit Ratio:**  $3/13 \approx 0,23$
- **Miss Ratio:**  $10/13 \approx 0,77$
- **Final Cache Contents:** Blocks 128, 17,74,211,21,7

### b- Fully Associative Cache with LRU

Time	0	1	2	3	4	5	6	7	8	9	10	11	12
Address	5469	2085	4126	675	4099	6755	2081	2370	8420	37	544	680	244
Block N° in MM	170	65	128	21	128	211	65	74	263	1	17	21	7
Block 0	<b>170</b>	<b>170</b>	<b>170</b>	<b>170</b>	<b>170</b>	<b>170</b>	<b>170</b>	<b>170</b>	<b>170</b>	<b>170</b>	<b>17</b>	<b>17</b>	<b>17</b>
Block 1		<b>65</b>	<b>65</b>	<b>65</b>	<b>65</b>	<b>65</b>	<b>65</b>	<b>65</b>	<b>65</b>	<b>65</b>	<b>65</b>	<b>65</b>	<b>65</b>
Block 2			<b>128</b>	<b>128</b>	<b>128</b>	<b>128</b>	<b>128</b>	<b>128</b>	<b>128</b>	<b>128</b>	<b>128</b>	<b>128</b>	<b>7</b>
Block 3				<b>21</b>	<b>21</b>	<b>21</b>	<b>21</b>	<b>21</b>	<b>21</b>	<b>21</b>	<b>21</b>	<b>21</b>	<b>21</b>
Block 4						<b>211</b>	<b>211</b>	<b>211</b>	<b>211</b>	<b>211</b>	<b>211</b>	<b>211</b>	<b>211</b>
Block 5								<b>74</b>	<b>74</b>	<b>74</b>	<b>74</b>	<b>74</b>	<b>74</b>
Block 6									<b>263</b>	<b>263</b>	<b>263</b>	<b>263</b>	<b>263</b>
Block 7										<b>1</b>	<b>1</b>	<b>1</b>	<b>1</b>
<b>Hit/miss</b>	<b>miss</b>	<b>miss</b>	<b>miss</b>	<b>miss</b>	<b>hit</b>	<b>miss</b>	<b>hit</b>	<b>miss</b>	<b>miss</b>	<b>miss</b>	<b>miss</b>	<b>hit</b>	<b>miss</b>

- **Hits:** 3
- **Misses:** 10
- **Hit Ratio:**  $3/13 \approx 0,23$
- **Miss Ratio:**  $10/13 \approx 0,76$
- **Final Cache Contents:** Blocks 7,17,65,7,21,211,74,263,1

### Exercise 2 : (6 pts)

1. **Structural Hazards:** Occur when a required hardware resource is busy and cannot service multiple instructions simultaneously.
  - **Techniques:** Resource duplication, pipeline stalls.
2. **Data Hazards:** Occur when an instruction depends on the result of a previous instruction that hasn't completed its data read/write operation yet. (RAW, WAR, WAW)
  - **Techniques:**
    - Insert "NOP"s (No Operation) in code at compile time
    - Rearrange code at compile time
    - Forward data at run time
    - Stall the processor at run time
3. **Control Hazards:** Occur when the pipeline must decide what instruction to fetch next, but that decision depends on a previous instruction (typically a branch) that hasn't completed yet.
  - **Techniques:** Branch prediction, delayed branches.

lw \$1,8(\$5)	IF	ID	EX	MEM	WB								
NOP		IF	ID	EX	MEM	WB							
add \$2, \$1, \$3			IF	ID	EX	MEM	WB						
beq \$2, \$1, Label				Stall	IF	ID	EX	MEM	WB				
lw \$4, 12(\$5)						IF	ID	EX	MEM	WB			
NOP							IF	ID	EX	MEM	WB		
sub \$2, \$3, \$4								IF	ID	EX	MEM	WB	

- Execution time= 12 Cycles

### Exercise 3 : (7 pts)

A)

1. **MIPS microprocessor family:** A family of Reduced Instruction Set Computer (RISC).
2. **FPU Co-processor role:** The Floating-Point Unit (Coprocessor 1) handles floating-point arithmetic operations (addition, subtraction, multiplication, division).

B)

Bkpt	Address	Code	Basic	Source
1	0x004000a8	0x34240018	ori \$4,\$1,24	
2	0x004000ac	0x0000000c	syscall	47: syscall
3	0x004000b0	0x24020001	addiu \$2,\$0,1	48: li \$v0, 1
4	0x004000b4	0x0109082a	slt \$1,\$8,\$9	49: for : ble \$t1,\$t0,label
5	0x004000b8	0x1020fff8	beq \$1,\$0,-8	
6	0x004000bc	0x000b2021	addu \$4,\$0,\$11	50: move \$a0,\$t3
7	0x004000c0	0x0000000c	syscall	51: syscall
8	0x004000c4	0x01483820	add \$7,\$10,\$8	52: add \$7,\$10,\$8
9	0x004000c8	0x0810002d	j 0x004000b4	53: j for
10	0x004000cc	0x112bfff9	beq \$9,\$11,-7	54: beq \$9,\$11,for
11	0x004000d0	0x032e6822	sub \$13,\$25,\$14	55: sub \$t5, \$t9, \$t6
12	0x004000d4	0x21290001	addi \$9,\$9,1	56: addi \$t1, \$t1, 1
13	0x004000d8	0x15ecffd0	bne \$15,\$12,-48	57: for2 : bne \$t7,\$t4,label2
14	0x004000dc	0x24090001	addiu \$9,\$0,1	58: li \$t1,1
15	0x004000e0	0x240a0000	addiu \$10,\$0,0	59: li \$t2,0

Instruction	Addressing mode
3	Immediate addressing
9	Pseudo-direct addressing
11	Register addressing
13	PC-relative addressing

Line10: `0x112BFFF9`

2. Effective Address:  $0x004000D0 - (0x0007 \ll 2) = 0x004000D0 - 0x001C = 0x004000B4$ .

Line 13: `0x15ECFFD0`

2. Effective Address:  $0x004000DC - (0x0030 \ll 2) = 0x00400034 - 0x00C0 = 0x0040001C$